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Configuration of Transceiver IC in Hand Held Radio for Military Purpose using FPGA

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Abstract: To configure a transceiver card for the hand held radio which is used for the transmission and reception of data or signals in war field. An RF Agile transceiver IC is an IC which is programmable is used. The IC is programmed to transmit and receive the signals in war field. The hand held radio system consists of baseband processor, FPGA on which the program is run to configure the transceiver card and has a flash memory where the programs to configure the transceiver at different frequencies are stored. As the radio is powered the respective programs stored in the flash memory is run on the FPGA based on the user data which is given as input, which will configures the transceiver IC in turn configuring the in-built analog and digital filters and the signal will be transmitted. Before transmitting the transceiver IC can be programmed for different modulation techniques depending on the user specifications.At the other radio same transceiver is used where the signal is received and is demodulated and processed to get the original message or signal.The simulation is done with the help of XILINX tool.

Keywords: Transceiver, FPGA, baseband processor.

I. INTRODUCTION

The hand held radios which were used earlier were using the RF components such as interpolation and decimation filters, analog-to-digital converter, digital-to-analog converter, local oscillator generator, power amplifiers. As all these components are included it resulted in a bulky system so to reduce the size of the entire system and make it compact the transceiver IC AD9361 is used. This IC has in-built RF components thus by programming this IC all the required RF components can be tuned to get the desired output.

There are several hand held radios which are used for military purpose which uses the RF components to fine tune the outputs they are:

[1]Type-1 multiband, multimission handheld radio in the field—the Harris AN/PRC-152

The Falcon III® AN/PRC-152 single-channel multiband, multimission handheld radio provides the optimal transition to JTRS technology. AN/PRC-152 satisfies the evolving mission requirements of war fighters by delivering secure, real-time information and communication at all points of need during coordination, combat, and crisis.

The features of this radio are 30-512 MHz multiband handheld, High Band option extending frequency range coverage to 30-520 MHz and 762-870MHz, Sierra programmable encryption, Supports SINCGARS, VHF/UHF AM and FM, and optional HAVEQUICK Optional APCO-P25 waveform for interoperability with civilian authorities,

Robust satellite tactical communications capability with advanced SATCOMS waveforms: SATCOM HPW messaging with (optional) IP data, JITC certified 181B up to 56 kbps, 182A/183A DAMA, Hardware configuration option, including embedded GPS receiver for situational awareness on the battlefield, and 20m Maritime versions (with or without GPS)

[2] The RF-5800M-HH multiband handheld radio

The RF-5800M-HH multiband handheld radio enables secure, reliable communications in missions ranging from standard squad operations to specialized forward air control and Special Forces. Covering the 30 to 512 MHz frequency range. The features of this radio are it offers a full suite of ECCM capabilities, now including the TALON waveform for secure ground-to-air communications, Intuitive user interface simplifies operation with push-to-talk voice communications available through the built-in speaker/microphone or the standard headset connector, External data interface enables connection to fielded PCs or other network data devices and integrated GPS provides simultaneous automated position reporting, Reliable, High-Performance Multiband Communications - Continuous coverage in the 30 to 512 MHz frequency band and up to 5 watts of output power for extended range capability, Software-Defined Platform - Enables upgrading to future waveforms, feature enhancements, or unique customer encryption algorithms, Extended Battery Life – combination of low power consumption architecture and high-capacity rechargeable Li-Ion battery ensures up to 18 hours of use, Rugged Design – Built to meet MIL-STD-810 specifications and endure immersion in up to 2 meters of water, with a 20 meter submersible version also available.

[3] THR9i

The THR9i is an advanced, versatile TETRA handheld radio. The features are Large QVGA colour display, Lifeguard – the advanced man-down alarm for user safety, IP65 class dust and water protection, Excellent battery performance, Configurable menu and short-cut

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keys, Voice feedback, Vibrating alert, Java TM MIDP 2.0 platform for applications.

[4] TGR990

The features of this hand held radio are Ergonomic CUR-3 control unit with Active TFT colour display, XHTML colour browser, Support for smart card-based end-to-end encryption (option), Java MIDP 2.0 platform for customized applications, Integrated GPS receiver.

[5] TMR880i

The features of this radio are integrated GPS receiver, Ergonomic CUR-3 control unit with ActiveTFT colour display, XHTML colour browser, Support for smart card-based end-to-end encryption (option), Java MIDP 2.0 platform for customized applications

[6] TGR980

3operation modes: Mobile radio, DMO Gateway, DMO Repeater, High-resolution TFT colour display, Integrated GPS receiver, Versatile installation options for a diverse range of vehicles, Advanced interfaces for external devices and applications.

[7] TMR880i

The features of this radio are Integrated GPS receiver, Ergonomic CUR-3 control unit with active TFT colour display, XHTML colour browser, Support for smart card-based end-to-end encryption (option), Java MIDP 2.0 platform for customized applications.

[8] TGR990

3 operation modes: Mobile radio, DMO gateway, DMO repeater, High-resolution TFT colour display, integrated GPS receiver, Advanced interfaces for the external devices and application.

II. PROPOSED MODEL

To configure a transceiver IC which is an AD9361 which is an integration of RF components for a hand held radio. Instead of using different filters, amplifiers, ADC's, DAC's and other circuits which results in bulk systems we can use an IC which has all the necessary RF components for transmission and reception of signals in-built in it. Just configuring the IC we can transmit and receive the signals and it also reduces the space consumed by the system.

The IC AD9361 is configured using an FPGA where the program is run to configure the registers which in-turn configures the required RF components to transmit and receive. The hand held radio which are developed previously were using separate analog and digital filters, analog-to-digital converters, digital-to-analog converters to process the signals from the baseband processor and the transmitting it using a transceiver module.

The transceiver modules are used only for the transmission and reception of signals and they don't have in-built filters for smoothing the signals which results in the bulk systems. Hence AD9361 transceiver IC is used which contains in-built RF components to process the signals and also it reduces overall size of the system.

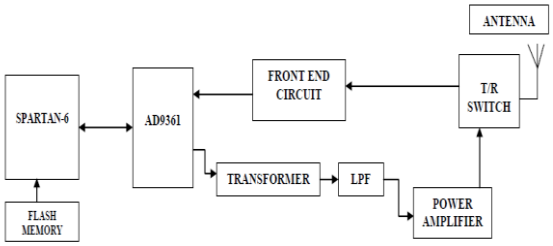

Fig. 1. General diagram of a hand held radio

The program to configure the AD9361 is stored in flash memory. When system is switched on depending on the user requirement the respective program is run on FPGA. Along with AD9361 we require some extra RF components as shown in the block diagram below. The antenna is used to transmit and receive the signals. T/R switch is used to decide the path i.e. whether the signal is to be transmitted or received. If the receiver path has to work then the switch is switched to receive mode.

After the switch the signal is passed through the front end circuit which comprises of following components; SPDT switch, Limiter, Coupler block, Control switches and Transformer.

Front End Circuit

This circuit is used to improve the receiver sensitivity and some filters are used to adjust the frequency between the required ranges.

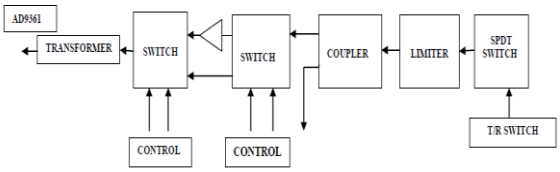

Fig. 2. Front End circuit

SPDT switch is used to provide about 60dB of isolation between the transmitter and receiver. Limiter is used to limit the power to 10dB as AD9361 works with 5dB input power and also it is used to protect the receiver with more power than limited.

Coupler comprises of a coupler, detector and comparator. This is used to determine whether to the power has to be amplified or not. As the comparator used DC signal we cannot give Ac signal directly to comparator so we are converting the power to equivalent voltage and then comparing whether to amplify are not.

The coupler is used so that the actual path is not disturbed. So that we will get a wide dynamic range. Transformer is used to convert the single ended input to differential input. At the transmitter path the transformer is used to convert the differential input to single ended input, low pass filter is used to suppress the harmonics and restricts the bandwidth. Power amplifier is used to increase the gain to 2W.

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III. AD9361 TRANSCEIVER

AD9361 Transceiver used in V/UHF Transceiver design is the heart of the system which provides frequency conversion from RF to IF frequency and vice versa. AD9361 Transceiver operates in the 70MHz to 6.0GHz range, covering most licensed and unlicensed bands channel band widths from less than 200 KHz to 56MHz.

Radio frequency (RF) Agile Transceiver designed for use in 3G and 4G base station applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines a RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor.

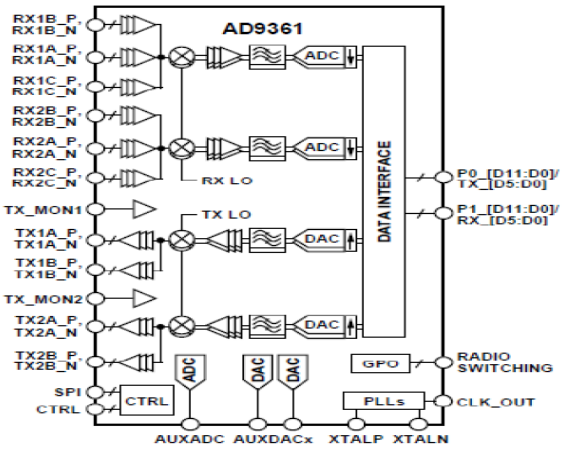

Fig.3 Functional block diagram of AD9361

Following are the major features of AD9361 that are available:

Feature	Description
Frequency band	70MHz – 6000MHz
Transceiver configuration	Supports TDD and FDD operation
Tunable output band width	<200KHz – 56MHz
Integrated fractional N-synthesizers	2.5Hz maximum local oscillator(LO) step size
Digital interface	CMOS/LVDS digital interface
No. of transmitter channels	Dual transmitter output with 4 diff. outputs
No. of Receiver channels	Dual receivers with 6 diff. or 12 single ended i/ps
Receiver sensitivity	Noise figure < 2.5dB
Output power	9dBm
Highly linear broad band transmitter	Tx EVM : ≤-40dB Tx noise : ≤-157dBm/Hz noise floor

The internal components of AD9361 are

At receiver side:

- Low noise amplifier (LNA)
- Local oscillator synthesizer
- Gain controller
- Analog filters
- Analog-to-digital converter
- Digital filters

At transmitter side:

- Low noise amplifier (LNA)
- Local oscillator synthesizer
- Gain controller
- Digital filters
- digital-to-Analog converter
- Analog filters

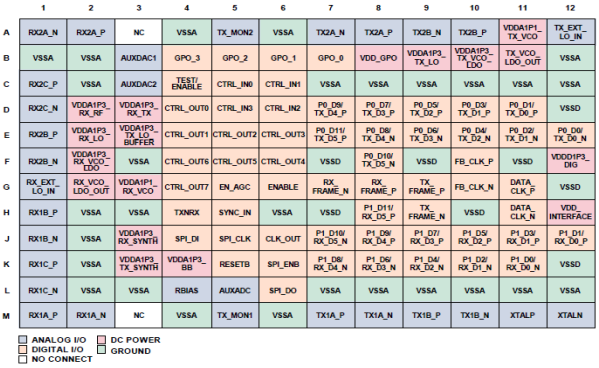

Fig.4 Pin Configuration and Function Descriptions

IV. RECEIVER

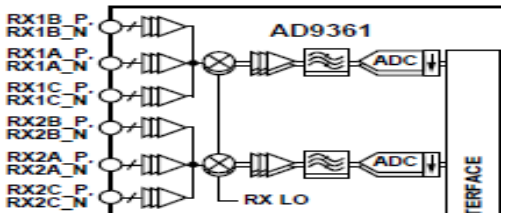

Fig.5 Receiver block diagram

The receiver section contains all blocks necessary to receive RF signals and convert them to digital data that is usable by a BBP. There are two independently controlled channels that can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer.

Each channel has three inputs that can be multiplexed to the signal chain, making the AD9361 suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a low noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that down convert received signals to baseband for digitization. External LNAs can also be interfaced to the device, allowing designers the flexibility to customize the receiver front end for their specific application.

Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed.

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Additionally, each channel contains independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self-calibration. The receivers include 12-bit, sigma-delta (Σ-Δ) ADCs and adjustable sample rates that produce data streams from the received signals.

The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

A. RX SIGNAL PATH

The AD9361 RX signal path passes down converted signals (I and Q) to the baseband receiver section. The baseband RX signal path is composed of two programmable analog low-pass filters, a 12-bit ADC, and four stages of digital decimating filters.

Each of the four decimating filters can be bypassed. The corner frequency for each low-pass filter is programmable via SPI registers. Figure 2 shows a block diagram for the AD9361 RX signal path. Note that both the I and Q paths are schematically identical to each other.

The digital RX HB filters are sized to eliminate over-ranging. The RX FIR filter can over-range based on the filter coefficients. The RX FIR output is limited to the maximum code value when over-ranging occurs (preventing data wrapping). An over-range occurrence in the RX FIR filter is indicated in registers 0x05E and 0x05F or at the CTRL_OUT pins when the control output pointer in register 0x035 is set to 0x0A. All adjustable RX filter settings are programmable via SPI registers.

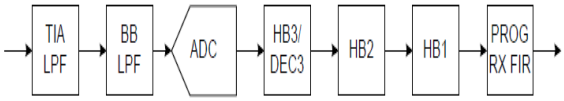

Fig.6 Rx signal path

V. TRANSMITTER

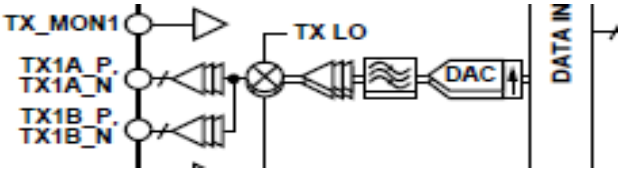

Fig.7 Transmitter block diagram

The transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter with interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for up conversion.

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the up conversion mixers. At this point, the I and Q signals are recombined and modulated on the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional band shaping, and then the signal is transmitted to the output amplifier. Each transmit channel provides a wide attenuation adjustment range with fine granularity to help designers optimize signal-to-noise ratio (SNR).

Self-calibration circuitry is built into each transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back through an unused receiver channel to the BBP for signal monitoring. The TX monitor blocks are available only in TDD mode operation while the receiver is idle.

A.TX SIGNAL PATH

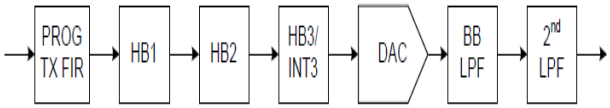

Fig.8 Tx signal path

The AD9361 TX signal path receives 12-bit 2s complement data in I-Q format from the AD9361 digital interface, and each channel (I and Q) passes this data through four digital interpolating filters to a 12-bit DAC. Each of the four interpolating filters can be bypassed.

The DAC's analog output is passed through two low pass filters prior to the RF mixer. The corner frequency for each low-pass filter is programmable via SPI registers.

VI. IMPLEMENTATION

Serial Peripheral Interface (Spi)

The SPI bus provides the mechanism for all digital control of the AD9361. Each SPI register is 8-bit wide, and each register contains control bits, status monitors, or other settings that control all functions of the device. The following sections explain the specifics of this interface.

Spi Functional Layer

The SPI bus can be configured by setting the bit values in SPI register 0x000. Register 0x000 is symmetrical; that is, D7 is equivalent to D0, D6 is equivalent to D1, and D5 is equivalent to D2 (D4 and D3 are unused). The device powers up in its default mode (MSB-first addressing), but can accept an LSB-first write to 0x000 because of this symmetry. The symmetrical bits are ORed together, so setting one bit sets both in the pair. The bit order is MSB-first when D5 and D2 are left clear, while bit order is swapped to LSB-first when these bits are

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set. Once properly configured, all subsequent register writes must follow the selected format.

The bus is configured as a 4-wire interface by default. If bits D6 and D1are set, the SPI bus is configured as a 3-wire interface. Bits D7 and D0 asynchronously reset all registers to their default values when set, and these bits must be cleared before other registers can be changed. The default state of register 0x000 is 0x00.

Spi Data Transfer Protocol

The AD9361 SPI is a flexible, synchronous serial communications bus allowing seamless interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel SSR protocols. The control field width for the AD9361 is limited to 16-bit only, and multi-byte IO operation is allowed. The AD9361 cannot be used to control other devices on the bus – it only operates as a slave.

There are two phases to a communication cycle. Phase 1 is the control cycle, which is the writing of a control word into the AD9361. The control word provides the AD9361 serial port controller with information regarding the data field transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 control field defines whether the upcoming data transfer is read or write. It also defines the register address being accessed.

The sensitivity of the system is analyzed based on the attenuation and bit error rate. From the analysis it is observed that up to a software attenuation of 62dB will receive the bits whatever we transmit after this value it results in bit error.

Timing Diagrams

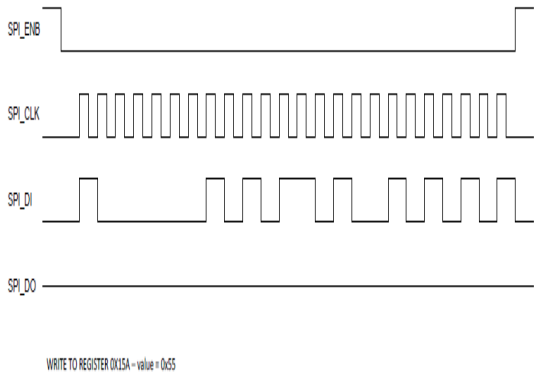

Fig.9 Nominal Timing Diagram, SPI Write

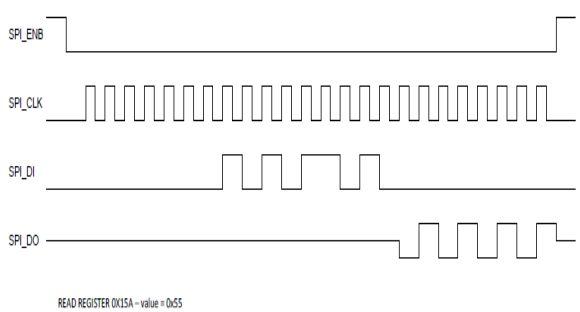

Fig.10 Nominal Timing Diagram, SPI Read

VII. ADVANTAGES, DISADVANTAGES AND APPLICATIONS

Advantages

- Precise tuning.
- Despite all the functions integrated into the part power consumption is generally around 1W.
- It is fully customizable in software without any hardware changes and provides additional options for various MIMO configurations
- It replaces a considerable amount of discrete circuitry, so the need for such discrete designs has been eliminated.

Disadvantages

- Writing a code to configure the IC is difficult.
- It is programmed for a specific FPGA family and the same program will not work for other families as the pin connection differs.

Applications

- Point to point communication systems
- Femtocell/picocell/microcell base stations
- General-purpose radio systems

VIII. CONCLUSION

Transceiver card for the hand held radio which is used for the transmission and reception of data or signals in war field is configured. The SPL read and write are verified and the sensitivitity of the system is checked.

IX. RESULTS

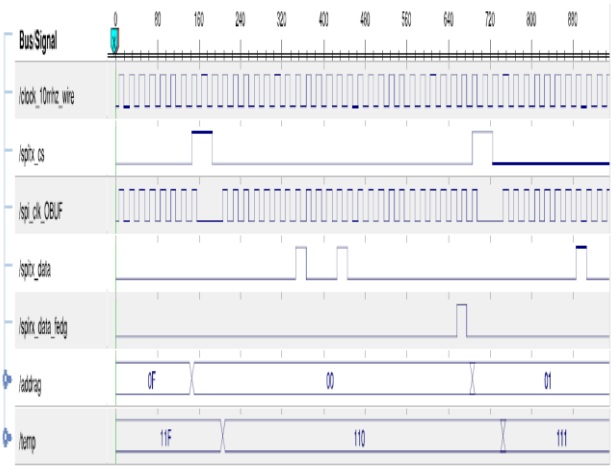

Fig.11 simulation result for Spi read

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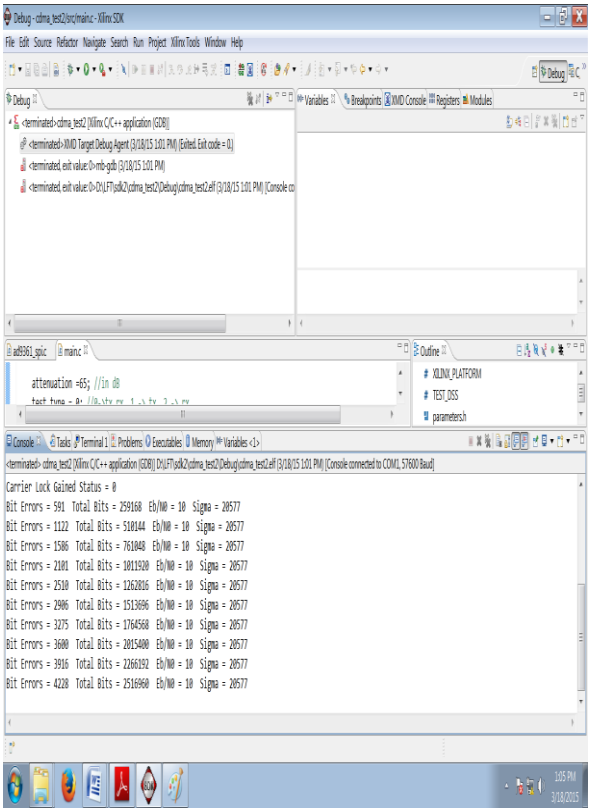

Fig.12 Bit errors for software attenuation=65

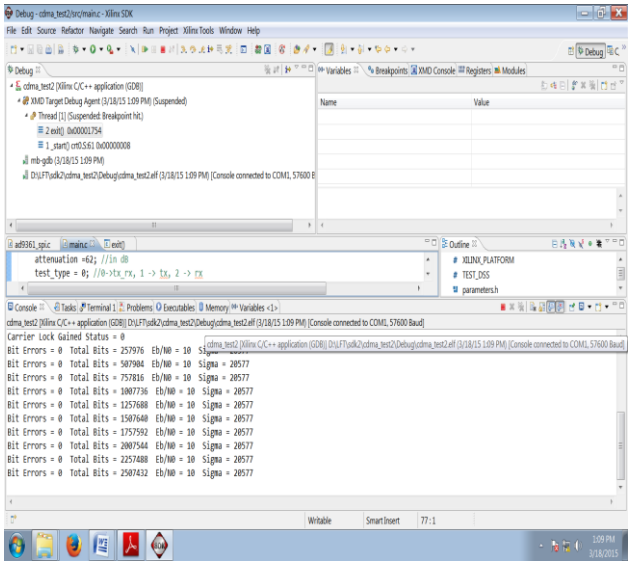

Fig.13 Bit errors for software attenuation=62

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